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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,865	10/30/2003	Michael Norman Day	AUS920030693US1	9752

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EXAMINER	
SCHELL, JOSEPH O	

ART UNIT	PAPER NUMBER
2114	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/697,865	DAY ET AL.	
	Examiner	Art Unit	
	Joseph Schell	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4 and 8-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11-20* is/are allowed.

6)☒ Claim(s) *1,2,4 and 8-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

Claims 1-2, 4, and 8-20 have been examined.

Claims 1-2, 4, and 8-10 have been rejected.

Claims 11-20 are allowable.

Response to Arguments

Applicant's arguments with respect to claims 1-10 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

Claims 11-20 are allowed. The following is a statement of reasons for the indication of allowable subject matter: Within claims 11, 15 and 18, within the entirety of each claim, the examiner deems the novel subject matter to be that the debugging processor dynamically allocates memory for the saved states, verifies halting of the supplemental processor, and restarts the supplemental processor.

Claim Objections

Claim 4 line 4 should include a comma to read "processor, comprising:"

Claim 8 line 3 should read "a secondary program in said first processor"

Claim 8, the last line states the limitation "the debugging process." This limitation lacks antecedent basis. The examiner recommends changing this limitation to read "the modifying step" or something similar.

Claim 10 line 4-5 should include a comma to read "activating a secondary program in a first processor, transmitting register states"

Claim 12 is improperly dependent on itself. The examiner is assuming claim 12 is instead dependent on claim 11 as the only independent method claim using "SPU" and "MPU" terminology.

Claim 18 line 9 should read "a copy program operation on the SPU, wherein the copy program is a computer program"

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-2, 4, and 8-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee (US Patent 6,484,274).

As per claim 1, Lee ('274) discloses a method, for use in a computer system having a main memory and a first processor, for providing said first processor with access to the register state of a supplemental processor (as shown in Figure 1 and discussed in the abstract, the CPU 110A is the supplemental and the monitor/development system 116 is the first processor), said supplemental processor otherwise inaccessible by said first processor (column 4 lines 3-5, only after saving the state to memory is control passed to the debugger), comprising:

loading a program into said supplemental processor (see abstract);

executing said program in said supplementary processor to generate said register states of said supplementary processor (see abstract);

storing said register state in said main memory (see abstract);

accessing said register state by said first processor (see abstract, error debugging is performed by loading the saved states in a development system); and

subsequent to storing said register states and accessing said register states, inspecting said register states for errors (see the last quarter of the abstract, the saved register states are examined)

As per claim 2, Lee ('274) discloses the method of claim 1 further including a program debugging operating on said main processor and wherein said method further includes:

accessing said register state in said main memory by said debugger to debug said program (column 3 lines 22-30).

As per claim 4, Lee ('274) discloses a method of debugging a specified program intended to operate on a supplemental processor, the register states of which cannot be directly accessed by a read command from another processor (column 4 lines 3-5) comprising:

reserving a pool of memory accessible to a debugging program processor (as shown in Figure 1A, separate memory area 130 is reserved for CPU states);

running a specified program, to be debugged, in said supplement processor until instructions in said specified program cause operation of said specified program to cease (column 2 lines 52-55);

activating a secondary program in said supplemental processor to transmit register states of said supplemental processor, at the time said specified program is operationally interrupted, to said debugging program processor (column 2 lines 61-65, a BIOS routine performs the state saving);

subsequent to transmitting said register states, inspecting said register states for errors (see abstract);

modifying parameters of said specified program in a memory pool accessible by said debugging program processor (column 3 lines 26-30); and

restoring operation of said specified program in said supplemental processor with modified parameters (column 6 lines 2-15 and as shown in Figure 2).

As per claim 8, Lee ('274) discloses a method of debugging a first processor unit employing a second processor operating a debugging program (a shown in Figure 1, the first processor is CPU 11A and the second is the monitor 116), comprising:

activating a secondary program in first processor to transmit register states of said first processor, said register states embodying program parameters (column 2 lines 61-66), subsequent to a time a specified program to be debugged is operationally interrupted, to said second processor (see abstract, after an error the state is saved and examined by the debugging processor);

subsequent to transmitting said register states, inspecting said register states for errors (see last quarter of abstract);

modifying parameters of said specified program in a memory pool accessible by said second processor through the use of said debugging program in said second processor (column 3 lines 26-30); and

restoring operation of said specified program in said first processor with alterations as created in the debugging process (column 6 lines 2-15).

As per claims 9 and 10, these claims recite limitations found in claim 4 and are rejected on the same grounds as claim 4.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Schell whose telephone number is (571) 272-8186. The examiner can normally be reached on Monday through Friday 9AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JS

SCOTT BADERMAN
SUPERVISORY PATENT EXAMINER